REMARKS

Claims 16-27 are pending in the Application. Claim 16 is an independent claim and claims 17-21 depend therefrom. Claim 22 is an independent claim and claims 23-27 depend therefrom. Claims 1-15 were previously canceled. Claims 16 and 22 are currently amended. The Applicant respectfully requests that the application be reconsidered in view of the foregoing amendments and the following remarks.

Rejections Under 35 U.S.C. §112, First Paragraph (Claims 16-27)

In point 2 on page 2 of the non-final Office Action, claims 16-27 were rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the written description requirement. (Office Action, Page 2). Specifically, the Office Action states that "[i]ndependent claim 16 has language which recites 'discrete components', as known in the electrical field of arts, such terminology refers to an electronic components with one circuit elements, which may be passive (resistor, capacitor…) or active (transistor) other than an integrated circuit." (Office Action, Page 2). However, as defined by Merriam-Webster's Online Dictionary, the term "discrete" is defined as "constituting a separate entity: individually distinct." (Merriam-Webster's Online Dictionary, "discrete," http://www.merriam-webster.com/dictionary/discrete). In other words, discrete components, as demonstrated by the Merriam-Webster definition and as clearly shown in the current application, indicates that the Applicant's video decoder is separate from its display engine. (*See e.g.*, Applicant's Figure 2 (video decoder 205 separate from display engine 210), Figure 5 (MPEG video decoder 545 separate from display engine 550), Figure 6 (separate video decoder 545), Figure 7 (separate display engine 550)). Regardless, in an effort to advance prosecution in the application, the Applicant has amended independent claims 16 and 22 to clarify that the video decoder and display engine are separate components. The Applicant notes that such amendment does not alter the scope of the claims in any way and respectfully requests that the rejection under 35 U.S.C. §112, first paragraph, be withdrawn.

Rejections Under 35 U.S.C. §103(a) – Wells in view of Choi (Claims 16-27)

In point 3 on pages 3-4 of the non-final Office Action, independent claims 16 and 22, and dependent claims 17-21 and 23-27 were rejected under 35 U.S.C. §103(a) as being unpatentable over Wells (U.S. Pat. Pub. No. 2004/0057624) in view of Choi (U.S. Patent No. 7,206,025). The Applicant respectfully traverses the rejection for at least the following reasons.

In order for a *prima facie* case of obviousness to be established, the Manual of Patent Examining Procedure, Rev. 6, Sep. 2007 ("MPEP") states the following:

> The key to supporting any rejection under 35 U.S.C. 103 is the clear articulation of the reason(s) why the claimed invention would have been obvious. The Supreme Court in KSR International Co. v. Teleflex Inc., 82 USPQ2d 1385, 1396 (2007) noted that the analysis supporting a rejection under 35 U.S.C. 103 should be made explicit. The Federal Circuit has stated that "rejections on obviousness cannot be sustained with mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness."

See the MPEP at § 2142, citing *In re Kahn*, 441 F.3d 977, 988, 78 USPQ2d 1329, 1336 (Fed. Cir. 2006), and *KSR International Co. v. Teleflex Inc.*, 82 USPQ2d at 1396 (quoting Federal Circuit statement with approval). Further, MPEP § 2143.01 states that "the mere fact that references can be combined or modified does not render the resultant combination obvious unless the results would have been predictable to one of ordinary skill in the art" (citing *KSR International Co. v. Teleflex Inc.*, 82 USPQ2d 1385, 1396 (2007)). Additionally, if a *prima facie* case of obviousness is not established, the Applicant is under no obligation to submit evidence of nonobviousness:

> The examiner bears the initial burden of factually supporting any *prima facie* conclusion of obviousness. If the examiner does not produce a *prima facie* case, the applicant is under no obligation to submit evidence of nonobviousness.

See MPEP at § 2142.

With regard to independent claim 16, the combination of Wells in view of Choi at least fails to describe, teach or suggest, for example, "a video decoder, said video decoder further comprising...a deinterlacer for deinterlacing the decompressed video data, thereby resulting in deinterlaced video data; and a display engine, said display engine comprising: a scalar for scaling the deinterlaced video data; wherein the video decoder and the display engine are separate components."

Similarly, with regard to independent claim 22, the combination of Wells in view of Choi at least fails to describe, teach or suggest, for example, "a video decoder, said video decoder further comprising...a deinterlacer connected to the decompression engine, the deinterlacer operable to deinterlace the decompressed video data, thereby resulting in deinterlaced video data; and a display engine connected to the video decoder, said display engine comprising: a scalar operable to scale the deinterlaced video data; wherein the video decoder and the display engine are separate components."

Wells teaches an integrated video decoding system that includes a decoder 202 and a post-processing stage 206. Wells' post-processing stage includes an integrated deblocking, temporal filtering and de-interlacing stage 208, and a shared memory 210. The Applicant notes that nowhere in Wells is there any disclosure of the de-interlacing occurring within the decoder 202 as opposed to in the integrated stage 208 of the post-processing stage 206. Further, nowhere in Wells is there any disclosure of the scaling occurring in a separate display engine after decompressing and deinterlacing in a video decoder.

With regard to scaling, certain embodiments of Wells discloses a scalar within the decoder 202. (*See, e.g.*, Wells, Paragraph [0043], Lines 16-19 and Paragraph [0048], Lines 3-7). In another embodiment of Wells, scaling is performed with de-interlacing. (*See, e.g.*, Wells, Paragraph [0051], Lines 1-5). The Applicant notes that in the above embodiments, Wells cannot teach "a video decoder, said **video decoder further comprising...a deinterlacer** for deinterlacing the decompressed video data, thereby resulting in deinterlaced video data; and a display engine, said **display engine comprising: a scalar for scaling the deinterlaced video**

data; wherein the video decoder and the display engine are discrete components," as recited in Applicant's independent claim 16 and similarly in Applicant's independent claim 22.

In yet another embodiment, Wells discloses that scaling is performed after temporal filtering and de-interlacing **in the single post-processing stage as opposed to within the decoder**. (*See e.g.*, Wells, Paragraph [0041], Lines 7-10). Thus, in the one embodiment where Wells teaches performing scaling after de-interlacing, Wells explicitly teaches that scaling is to be done in the single post-processing stage that includes the deinterlacing and is separate from the decoder in order to improve system efficiency. Thus, Wells teaches away from including the post-processing stage 206 within the decoder 202 by toting the advantages (i.e., improved system efficiency) of having a single post-processing stage that includes deblocking, scene classification, temporal filtering, deinterlacing and scaling. (Wells, Paragraphs [0039]-[0041]).

With regard to Wells' de-interlacer, each of the decoding systems disclosed in Wells teaches a separate video decoder coupled to a separate post-processing stage. Further, the de-interlacer in each of the decoding systems disclosed in Wells is separate from the video decoder and is instead part of the post-processing stage.

Additionally, Wells teaches away from moving the de-interlacer from the post-processing stage into the video decoder for at least two reasons. First, Wells teaches saving system cost and processing latency by combining the deblocking, (MC) temporal filtering and (MC) de-interlacing into a single stage so that the motion vector, scene cut, and scene classification information can be shared by all post processing tasks. (*See* Wells, Paragraphs [0039]-[0040]). Thus, to realize the advantages of the Wells decoding system, Wells teaches away from removing the de-interlacer of Wells from the post-processing stage and adding the de-interlacer to the video decoder. Second, Wells sets forth in an alternative embodiment, adding the deblocker to the decoder because, although it would "require[] a more expensive and capable decoder, information in the compressed bitstream itself can be used to improve deblocking." (Wells, Paragraph [0043]). However, Wells fails to disclose alternative embodiments for adding the (MC) temporal filter and/or (MC) de-interlacer to the video decoder. By setting forth an alternative embodiment for adding the deblocker to the decoder but not disclosing alternative

embodiments for adding the (MC) temporal filter and/or the (MC) de-interlacer to the decoder, Wells clearly intended for the de-interlacer to be integrated in the post-processing stage separate from the video decoder to realize the system cost and processing latency savings of the Wells decoding system.

Choi fails to remedy the deficiencies of Wells. Choi, which is silent with regard to deinterlacing and scaling, appears to be cited for the purpose of integrating Wells' post-processing stage 206 into Wells' decoder 202. However, the Applicant's independent claims 16 and 22 recite "**wherein the video decoder and the display engine are discrete components**." In other words, Choi's teaching of integrating components teaches away from Applicant's discrete video decoder and display engine. Further, as discussed above, Wells' teaches away from integrating the single post-processing stage 206 into the decoder 202. Additionally, even if Wells' post-processing stage 206 was integrated into Wells' decoder 202, Wells' scaling function would also become integrated into the decoder. In other words, the combination of Wells and Choi cannot disclose "a video decoder, said **video decoder further comprising**...**a deinterlacer** for deinterlacing the decompressed video data, thereby resulting in deinterlaced video data; and a display engine, said **display engine comprising**; **a scalar for scaling the deinterlaced video data**; **wherein the video decoder and the display engine are discrete components**," as recited in Applicant's independent claim 16 and similarly in Applicant's independent claim 22.

Also, if the non-final Office Action is asserting that the combination of Wells and Choi discloses adding the post-processing stage into the video decoder (which it does not), then Wells would at least fail to disclose "a display engine, said display engine comprising: a scalar for scaling the deinterlaced video data; wherein the video decoder and the display engine are discrete components," at least because Wells teaches "the post-processing stage further integrates format conversion and scaling functions...." (Wells, Paragraph [0041]).

The Office Action appears to allege that whether various components are separate or integrated, and the order of the components is unimportant; however, the Applicant notes that

such features are critical to the Applicant's invention. Specifically, as discussed in Paragraphs [0008]-[0009] of the Applicant's Specification:

> In conventional system, the deinterlacer deinterlaces interlaced frames after scaling, and very close to the presentation time on the display unit.
>
> Deinterlaced interlaced frames close to the presentation time is disadvantageous for number of reasons. Because the interlaced frames are scaled before interlacing, the scaler individually scales each field of the interlaced frames, without regard for the additional video data in the other field of the interlaced frame. Additionally, deinterlacing interlaced frames involves considerable real-time processing.

(Applicant's Specification, Paragraphs [0008]-[0009]). As shown above, it is critical to performing scaling separate from and after deinterlacing so that deinterlacing occurs as early as possible and for increasing the effectiveness of the scaling. In contrast and as discussed above, Wells teaches either performing scaling before deinterlacing or with deinterlacing and separate from the decoder to improve system efficiency. Thus, these critical aspects of the Applicant's invention are explicitly taught away from in Wells.

Therefore, for at least the reasons set forth above, the Applicant respectfully submits that the Office Action's assertion that Applicant's claims 16-27 are unpatentable over Wells in view of Choi under 35 U.S.C. §103(a), amounts to clear error at least because the combination of Wells and Choi fails to disclose "a video decoder, said **video decoder further comprising**...**a deinterlacer** for deinterlacing the decompressed video data, thereby resulting in deinterlaced video data; and a display engine, said **display engine comprising**: **a scalar for scaling the deinterlaced video data**; **wherein the video decoder and the display engine are discrete components**."

For at least the reasons set forth above, the Applicant respectfully asserts that independent claims 16 and 22 are allowable over Wells in view of Choi. The Applicant requests that the rejection of claims 16 and 22 under 35 U.S.C. §103(a), be withdrawn.

Because dependent claims 17-21 and 23-27 depend, directly or indirectly, from independent claims 16 and 22, respectively, and because claims 16 and 22 are allowable over

Wells in view of Choi, the Applicant asserts that claims 17-21 and 23-27 are also allowable over Wells in view of Choi. The Applicant also submits that each of claims 17-21 and 23-27 is independently allowable as well. Therefore, the Applicant requests that the rejection of claims 17-21 and 23-27 under 35 U.S.C. §103(a), be withdrawn.

Final Matters

The non-final Office Action makes various statements regarding claims 16-27, 35 U.S.C. § 112, first paragraph, 35 U.S.C. § 103(a), the Wells reference, the Choi reference, one of ordinary skill in the art, etc. that are now moot in view of the above amendments and/or arguments. Thus, the Applicant will not address all of such statements at the present time. However, the Applicant expressly reserves the right to challenge such statements in the future should the need arise (e.g., if such statements should become relevant by appearing in a rejection of any current or future claim).

Applicant reserves the right to argue additional reasons supporting the allowability of claim 16-27 should the need arise in the future.

CONCLUSION

Applicant respectfully submits that that all of claims 16-27 are in condition for allowance, and requests that the application be passed to issue.

Should anything remain in order to place the present application in condition for allowance, the Examiner is kindly invited to contact the undersigned at the telephone number listed below.

Please charge any required fees not paid herewith or credit any overpayment to the Deposit Account of McAndrews, Held & Malloy, Ltd., Account No. 13-0017.

Dated: December 29, 2009

Respectfully submitted,

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